SYLLABUS
MASTER OF TECHNOLOGY PROGRAMME IN VLSI DESIGN (4 SEMESTERS) REGULATIONS 2010
SATHYABAMA UNIVERSITY
REGULATIONS – 2010

Effective from the academic year 2010-2011 and applicable to the students admitted to the Master of Engineering / Technology / Architecture / Science (Four Semesters)

1. Structure of Programme

   1.1 Every Programme will have a curriculum with syllabi consisting of theory and practical such as:
      (i) General core courses like Mathematics
      (ii) Core course of Engineering / Technology/Architecture / Science
      (iii) Elective course for specialization in related fields
      (iv) Workshop practice, Computer Practice, laboratory Work, Industrial Training, Seminar Presentation, Project Work, Educational Tours, Camps etc.

   1.2 Each semester curriculum shall normally have a blend of lecture course not exceeding 7 and practical course not exceeding 4.

   1.3 The medium of instruction, examinations and project report will be English.

2. Duration of the Programme

   A student is normally expected to complete the M.E/M.Tech./M.Arch/M.Sc Programme in 4 semesters but in any case not more than 8 consecutive semesters from the time of commencement of the course. The Head of the Department shall ensure that every teacher imparts instruction as per the number of hours specified in the syllabus and that the teacher teaches the full content of the specified syllabus for the course being taught.

3. Requirements for Completion of a Semester

   A candidate who has fulfilled the following conditions shall be deemed to have satisfied the requirement for completion of a semester.

      3.1 He/She secures not less than 90% of overall attendance in that semester.

      3.2 Candidates who do not have the requisite attendance for the semester will not be permitted to write the University Exams.

4. Examinations

   The examinations shall normally be conducted between October and December during the odd semesters and between March and May in the even semesters. The maximum marks for each theory and practical course (including the project work and Viva Voce examination in the Fourth Semester) shall be 100 with the following breakup.

   (i) Theory Courses

      Internal Assessment : 20 Marks
      University Exams : 80 Marks

   (ii) Practical courses

      Internal Assessment : - -
      University Exams : 100 Marks
5. **Passing requirements**

(i) A candidate who secures not less than 50% of total marks prescribed for the course (For all courses including Theory, Practicals and Project work) with a minimum of 40 marks out of 80 in the University Theory Examinations, shall be declared to have passed in the Examination.

(ii) If a candidate fails to secure a Pass in a particular course, it is mandatory that he/she shall reappear for the examination in that course during the next semester when examination is conducted in that course. However the Internal Assessment marks obtained by the candidate in the first attempt shall be retained and considered valid for all subsequent attempts.

6. **Eligibility for the Award of Degree**

A student shall be declared to be eligible for the award of the M.E/M.Tech./M.Arch./M.Sc degree provided the student has successfully completed the course requirements and has passed all the prescribed examinations in all the 4 semesters within the maximum period specified in clause 2.

7. **Award of Credits and Grades**

All assessments of a course will be done on absolute marks basis. However, for the purpose of reporting the performance of a candidate, Letter Grades will be awarded as per the range of total marks (out of 100) obtained by the candidate as given below:

<table>
<thead>
<tr>
<th>RANGE OF MARKS FOR GRADES</th>
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</thead>
<tbody>
<tr>
<td>Range of Marks</td>
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<tr>
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</tr>
<tr>
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<td>00-49</td>
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**CUMULATIVE GRADE POINT AVERAGE CALCULATION**

The CGPA calculation on a 10 scale basis is used to describe the overall performance of a student in all courses from first semester to the last semester. F and W grades will be excluded for calculating GPA and CGPA.

\[
CGPA = \frac{\sum C_i GP_i}{\sum C_i}
\]

where \( C_i \) - Credits for the subject

\( GP_i \) - Grade Point for the subject

\( \Sigma_i \) - Sum of all subjects successfully cleared during all the semesters
8. Classification of the Degree Awarded

1. A candidate who qualifies for the award of the Degree having passed the examination in all the courses of all the semesters in his/her first appearance within a maximum period of 4 consecutive semesters after commencement of study securing a CGPA not less than 9.0 shall be declared to have passed the examination in First Class – Exemplary.

2. A candidate who qualifies for the award of the Degree having passed the examination in all the courses of all the semesters in his/her first appearance within a maximum period of 4 consecutive semesters after commencement of study, securing a CGPA not less than 7.5 shall be declared to have passed the examination in First Class with Distinction.

3. A candidate who qualifies for the award of the Degree having passed the examination in all the courses of all the semesters within a maximum period of 4 consecutive semesters after commencement of study securing a CGPA not less than 6.0 shall be declared to have passed the examination in First Class.

4. All other candidates who qualify for the award of the Degree having passed the examination in all the courses of all the 4 semesters within a maximum period of 8 consecutive semesters after his/her commencement of study securing a CGPA not less than 5.0 shall be declared to have passed the examination in Second Class.

5. A candidate who is absent in semester examination in a course/project work after having registered for the same, shall be considered to have appeared in that examination for the purpose of classification of degree. For all the above mentioned classification of Degree, the break of study during the programme, will be counted for the purpose of classification of degree.

6. A candidate can apply for revaluation of his/her semester examination answer paper in a theory course, within 1 week from the declaration of results, on payment of a prescribed fee along with prescribed application to the Controller of Examinations through the Head of Department. The Controller of Examination will arrange for the revaluation and the result will be intimated to the candidate concerned through the Head of the Department. Revaluation is not permitted for practical courses and for project work.

Final Degree is awarded based on the following:

- CGPA $\geq 9.0$ - First Class - Exemplary
- CGPA $7.50 < 9.0$ - First Class with Distinction
- CGPA $6.00 < 7.50$ - First Class
- CGPA $5.00 < 6.00$ - Second Class

Minimum CGPA requirements for award of Degree is 5.0 CGPA.

9. Discipline

Every student is required to observe disciplined and decorous behaviour both inside and outside the University and not to indulge in any activity which will tend to bring down the prestige of the University. If a student indulges in malpractice in any of the University theory / practical examination, he/she shall be liable for punitive action as prescribed by the University from time to time.

10. Revision of Regulations and Curriculum

The University may revise, amend or change the regulations, scheme of examinations and syllabi from time to time, if found necessary.
### M.Tech – VLSI DESIGN

#### REGULATIONS 2010 – CURRICULUM

#### SEMESTER I

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>SUBJECT CODE</th>
<th>SUBJECT TITLE</th>
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<tr>
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**Total Credits: 18**

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**Total Credits: 18**

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L - Lecture Hours; T - Tutorial Hours; P - Practical Hours; C - Credits
UNIT I ID TRANSFORMS


UNIT II 2D TRANSFORMS


UNIT III WAVELET TRANSFORMS


UNIT IV PROBABILITY & RANDOM VARIABLES

Probability concepts- Random variable - moment generating function - discrete types, continues types -2D variable random variables – marginal, conditional, joint probability distribution - Binomial, Poisson, uniform, normal and Exponential distributions

UNIT V RANDOM PROCESS


TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
(Distribution may be 40% Theory & 60% Problem)
UNIT I SEQUENTIAL LOGIC CIRCUITS  
Mealy machine, Moore machine, Trivial/Reversible/Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in fundamental and pulse mode.

UNIT II SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN  
Analysis of clocked synchronous sequential Networks (CSSN), Modeling of CSSN-State table assignment and reduction – Design of CSSN-Design of iterative circuits- ASM Chart- ASM Realization.

UNIT III ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN  
Analysis of Asynchronous sequential Circuits (ASC)-Flow table reduction -Races in ASC State assignment-Problem and the Transition table-Design of ASC-Static and Dynamic hazards-Data synchronizers-Designing of Vending machine controller-Mixed operating mode Asynchronous circuits.

UNIT IV PROGRAMMABLE LOGIC DEVICES  
Basic concepts, programming technologies, Programmable Logic Element(PLE),Programmable Logic Array(PLA),Programmable Array Logic(PAL),Structure of standard PLD’s, Complex PLD’s(CPLD)-System design using PLD’s-Design of combinational and sequential circuits using PLD’s, Programmable PAL device using PALASM, Design of state machine using Algorithmic State Machines(ASM) chart as design tool.

UNIT V STUDY OF FPGA AND XILINX  
Introduction to Field Programmable Gate Arrays-Types of FPGA –Xilinx XC3000 series, Logic Cell Array(LCA),Configurable Logic Blocks(CLB),Input/Output Block(IOB)-Programmable Interconnect Point(PIP),Introduction to ACT2 family and Xilinx XC4000 families, Design examples.

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN
Max. Marks: 80  
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice  
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks  
(Distribution may be 40% Theory & 60% Problem)
UNIT I

10 hrs.

Review of MOS electrical properties – Expression for threshold voltage and drain current - Energy band structure and band bending in the different region of operation - Secondary effects of MOSFET-review of CMOS and bipolar technologies.

UNIT II

10 hrs.

Basic inverter - Inverter Device sizing - Enhancement load and Depletion load inverters – CMOS inverter – CMOS inverter logic levels – Inverter device sizing – combinational logic implementation using NMOS and CMOS inverters - NMOS and CMOS design rules – stick diagram and layout.

UNIT III

10 hrs.

Steering logic design – programmable logic arrays – Folded PLA's – structured gate arrays – Dynamic MOS storage circuits – performance of Dynamic logic – clocked CMOS logic

UNIT IV

10 hrs.

CMOS static flip flops - dynamic sequential circuits – CMOS Logic – NORA CMOS - True single phase clocked logic – Capacitors and performance in CMOS – driving large capacitance - Resistance and performance

UNIT V

10 hrs.

Design of addres: Static, Dynamic, Manchester carry chain, Carry bypass adder, CSA, Carry look ahead adder –Multipliers : Baugh wooley, Booth Multiplier – Barrel shifter – NOR and NAND ROMs – operations in CMOS SRAM – Sence amplifiers

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80 Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice. 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
(Distribution may be 75% Theory & 25% Problem)
UNIT I

Overview of MOS: Characteristics of a MOS transistor - Surface properties of Silicon: Energy band diagram for the ideal case - Calculation of the threshold voltage \( v_T \) - Non ideal effects - CV plots: importance - Ideal case - High frequency CV plots - Low Frequency CV plots - Equations to CV plots - Deep depletion - Deviations from the Ideal CV plots - Interface traps, Effect of AC signal on the interface states - Techniques to measure \( C_{it} \), computation of \( C_S \) and \( P_S \) - Limitation in high frequency techniques - Comparison of measurements at high and low frequency techniques.

UNIT II

Sources of oxide trapped charge - Radiation created oxide trapped charge - Experimental results - How oxide trapped charge can be annealed out - models to explain the technique - Shifts in threshold voltage in P-channel and N-channel MOSFET - Disadvantages - Shifts at dynamic bias - Radiation hardening - Other alternatives dielectrics - gate metallization

UNIT III

MOSFET - Parameters of importance - Qualitative analysis of MOSFET - Mathematical model of IV characteristics - SPICE level1, level2, level3 models - Change in velocity with electric field - Expression for \( I_D \) in the sub threshold region of operation.

UNIT IV

Non uniform doping and effect on threshold voltage - Short channel effect - Narrow width effect - Small geometry effects - Shrink and Scaling. Small signal analysis of MOSFET - Derivation of the different parameters associated with the small signal model - Cutoff frequency - Hot carrier effects - 1988 model - Monte Carlo analysis

UNIT V

MOSFET devices - HMOS, DMOS, DIMOS, UMOS, VMOS, Sy MOSFET, SOS, Si MOX, BESOI, SEU, FAMOS, MCOS - Comparison with the conventional CMOS. MOS Device application: Depletion mode device - MOSFET connected as load devices - MOSFET as resistors, Static protection.

TEXT BOOK:


REFERENCE BOOKS:


UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80
Exam Duration: 3 hrs.
Part A: 6 Questions of 5 marks each - No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION.  

UNIT II LITHOGRAPHY AND RELATIVE PLASMA ETCHING 

UNIT III DEPOSITION, DIFFUSION , ION IMPLANTATION AND METALIZATION 

UNIT IV METALLIZATION 

UNIT V ANALYTICAL , ASSEMBLY TECHNIQUES & PACKAGING OF VLSI DEVICES 

TEXT BOOK: 

REFERENCES BOOKS: 

UNIVERSITY EXAM QUESTION PAPER PATTERN 
Max. Marks: 80  
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks

M.Tech (VLSI DESIGN)  5  REGULATIONS 2010
UNIT I SPECTRUM ESTIMATION & PREDICTION  

UNIT II ADAPTIVE FILTERS  

UNIT III MULTI RATE SIGNAL PROCESSING  
Mathematical description of change of sampling rate- interpolation- decimation- continuous time model- direct digital domain approach- decimation by an integer factor- interpolation by an integer factor- single and multi stage realization-poly phase realision- filter bank implementation- application to sub band coding.

UNIT IV IMAGE ENHANCEMENT AND RESTORATION  

UNIT V IMAGE DATA COMPRESSION  

TEXT BOOK:  

REFERENCE BOOKS:  

UNIVERSITY EXAM QUESTION PAPER PATTERN  
Max. Marks: 80  
Exam Duration : 3 hrs.  
Part A: 6 Questions of 5 marks each – No choice  
30 marks  
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks.  
50 marks  
(Distribution may be 70% Theory & 30% Problem)
UNIT I SINGLE STAGE AMPLIFIERS AND CURRENT MIRRORS
10 hrs.


UNIT II OP AMP DESIGN AND ADVANCED CURRENT MIRRORS
10 hrs.

Two stage CMOS op amp – op amp as a comparator – Charge injection errors, Latched Comparators – Advanced current mirrors – folded cascade and current mirror op amp – Linear settling time revisited, fully differential op amp - Analysis of Differential Amplifier with active load, supply and temperature independent biasing techniques.

UNIT III VOLTAGE REFERENCE, SAMPLE AND HOLD CIRCUITS
10 hrs.


UNIT IV DATA CONVERTERS AND NEURAL INFORMATION PROCESSING
10 hrs.


UNIT V SWITCHED CAPACITOR CIRCUITS AND PLL
10 hrs.


TEXT BOOKS:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80
Exam Duration : 3 hrs.

Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I INTRODUCTION

UNIT II LOGIC OPTIMIZATION

UNIT III OVERVIEW ON TOOLS FOR LAYOUT

UNIT IV FLOOR PLANNING AND PLACEMENT TECHNIQUES

UNIT V VERIFICATION AND CIRCUIT EXTRACTION
Ordered binary decision diagram : Operation, synthesis OBDDs. Paradigmatic application of OBDDs. Optimization of variable ordering Compaction : Problem formulation, Classification, One dimensional compaction, Hierarchical Compaction, Recent trends – Applications of VLSI circuits.

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN
Max. Marks: 80
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks each. 50 marks
(Distribution may be 90% Theory & 10% Problem)
UNIT I 10 hrs.


UNIT II 10 hrs.

Retiming – definition and properties, solving systems of inequalities, Retiming techniques – Unfolding –Properties and algorithm for unfolding, critical path and applications of unfolding – folding transformation, register minimization technique, register minimization in folded architectures - folding of multi rate systems

UNIT III 10 hrs.

Systolic architecture design – methodology, FIR systolic array, selection of scheduling vector , matrix to matrix multiplication , 2D systolic array design, systolic design for space representation containing delays – fast convolution algorithms – Redundant arithmetic - carry free radix 2 addition and subtraction - Radix 2 hybrid redundant multiplication architectures - data format conversion - Redundant to non-redundant converter -Numerical strength reduction.

UNIT IV 10 hrs.

Bit level arithmetic structures- parallel multipliers - interleaved floor plan and bit plan based digital filters - Bit serial multipliers. Bit serial filter design and implementation - Canonic signed digit arithmetic - Distributed arithmetic- Synchronous pipelining and clocking styles - clock skew and clock distribution in bit level pipelined VLSI designs - Wave pipelining - constraint space diagram and degree of wave pipelining - Implementation of wave-pipelined systems - Asynchronous pipelining – Schur algorithm .

UNIT V 10 hrs.

Design of VLSI Architectures for Digital Signal Processing- Architectural Design at Register Transfer Level - Design of Datapath elements Control structures Testable and self-reconfigurable fault-tolerant structures - Speed-Area-Power tradeoff Issues related to mixed signal design and SoC - CORDIC algorithm and multiplier less architectures - Scaling versus power consumption.

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80 Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice  30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks  50 marks
(Distribution may be 30% Theory & 70% Problem)
UNIT I 10 hrs.
Introduction- Need for Low power VLSI design– Charging and Discharging Capacitance- Short circuit current in CMOS- CMOS leakage current- Static current- Principles of Low power design- Low power figure of Merits.

UNIT II 10 hrs.
Simulation power analysis- SPICE circuit analysis- Discrete Transistor Modeling and analysis - Gate Level Logic simulation - Architecture level analysis - Data Correlation analysis in DSP systems - Monte Carlo Simulation - Random Logic signal- Probability Power analysis techniques- Signal entropy.

UNIT III 10 hrs.
Transistor and gate sizing- Network Restructuring and Reorganization- special latches and Flip flops-Low power digital cell library - Gate Reorganization- Signal Gating –Logic Encoding -State Machine encoding- Precomputation Logic.

UNIT IV 10 hrs.

UNIT V 10 hrs.
Advanced techniques- Adiabatic Computation- Pass transistor Logic synthesis -Asynchronous circuits - Software Design for Low power-Sources of software power dissipation- Software power optimization.

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN
Max. Marks: 80 Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I INTRODUCTION

UNIT II FAILURES AND FAULTS

UNIT III TESTING OF SEQUENTIAL CIRCUITS
Test generation for sequential circuits – State table verification - functional fault model – Equivalence Checking - Level sensitive scan design – Clocked Hazard free latches – Arithmetic and Reed Muller Coefficients - Software and Hardware Fault Tolerance.

UNIT IV BUILT-IN SELF-TEST (BIST)
Test pattern generation for built in self test. Exhaustive pattern generation and deterministic testing - Output response Analysis – Transition count syndrome checking Signature Analysis – Circular BIST.

UNIT V TESTABLE MEMORY DESIGN
RAM fault model – Test algorithm for RAMs. GALPAT – March Test – Detection of pattern sensitive faults- built in self test techniques for RAM chips. Self testable SRAM architecture. Test generation and BIST for Embedded RAMs Case study:- Online testing approach for very deep submicron ICs.

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN
Max. Marks: 80
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice  30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks  50 marks
(Distribution may be 80% Theory & 20% Problem)
EDA TOOLS LABORATORY  
(Common to VLSI, NanoTech)  

<table>
<thead>
<tr>
<th>Credits</th>
<th>Total Marks</th>
</tr>
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<tbody>
<tr>
<td>4</td>
<td>100</td>
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Analog Experiments

I. To acquire the knowledge of designing and simulation of basic analog circuits using Pspice

1. Analog amplifiers.
2. Oscillators
3. BJT biasing circuits
4. FET characteristics
5. Multivibrators
6. RLC circuits
7. Passive filters
8. Attenuators
9. Electrical circuit theorems
   1. Superposition Theorem
   2. Maximum power transfer theorem
   3. Norton’s Theorem
   4. Reciprocity Theorem
10. Waveform Generation Circuits
    1. Schmitt Trigger
    2. Square wave Generator
    3. Switch mode power supply (SMPS)
    4. Schmitt Trigger
11. Diode Experiments
12. Modulation Circuits
13. Op- amps

Digital Experiments

14. Combinational Circuits
15. Sequential Circuits
16. Inverters with various types of load
17. Scaling of MOS devices

II. Preparation of Layouts using MAGIC.

For all experiments shown above, the VLSI layout would be prepared by using the tool MAGIC.
LIST OF EXPERIMENTS

I. Verilog / VHDL Simulation, Synthesis & FPGA implementation of
   1. 4 bit Adders & Subtractors (CLA, CSA, CMA, Parallel adders)
   2. Design of FF (SR, D, T, JK, Master Slave with delays)
   3. Design of code converters & Comparator
   4. Design of Encoder, Decoder, Multiplexer, and De multiplexer
   5. Design of registers using latches and flip-flops
   6. Design of 8 bit Shift registers
   7. Design of Asynchronous & Synchronous Counters
   8. Modeling of Moore & Mealy FSM
   9. Static & Rolling Display
   10. Frequency Multipliers & Dividers
   11. Design of ALU
   12. Barrel Shifters
   13. Key Scan
   14. 4 bit Microprocessor
   15. RISC CPU
   16. Traffic light controller
   17. Design of memories
   18. Design of MAC unit
   19. Design of Sorting Circuit
   20. Design of FSM

II. Design Project Laboratory
   To get a basic knowledge about the FPGA and ASIC flow
   1. Layout Preparation for basic gates, adders, MUX and Flip flops
   2. Layout Preparation for the combinational circuits using MUX
   3. Layout Preparation for sequential circuits using Flip flops (Counters & registers)
   4. Architecture development and layout preparation for Sine Wave generation
   5. FPGA implementation and layout preparation for
      a. Two stage Op Amp.   b. Voltage controlled Oscillator
      c. A/D and D/A converters  d. 8 bit Microprocessor
      e. Traffic light Controller  f. Peripheral Devices
      g. Low noise Amplifier   h. Filter Design
UNIT I BASIC CONCEPTS IN VHDL
10 hrs.

UNIT II MODELING AND FEATURES IN VHDL
10 hrs.
Data flow modeling – Structural modeling – Behavioral modeling - Modeling a test bench – Generics and configurations- Sub programs - Hardware modeling examples : Moore FSM, Mealy FSM.

UNIT III VERILOG HDL
10 hrs.
Basic concepts – Module – Delays - Language elements – Compiler directives, value set, data types, Parameters – Expressions - Operands & operators - Gate level modeling – User defined Primitives – Combination UDP, Sequential UDP.

UNIT IV MODELING AND FEATURES IN VERILOG HDL
10 hrs.

UNIT V SYSTEM VERILOG
10 hrs.
Introduction to system verilog - Data types, Arrays, operators & Expressions - procedural & control flow statements - process, tasks & functions - Random constraints - Interprocess synchronization and communication - clocking blocks & program blocks - Interfaces & Mod ports

TEXT BOOKS:
1. J.Bhasker "VHDL Primer ", Prentice Hall, 1999

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN
Max. Marks: 80 Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I INTRODUCTION

Embedded system- characteristics of embedded system- categories of embedded system- requirements of embedded systems- challenges and design issues of embedded systems- trends in embedded systems- system integration- hardware and software partition- applications of embedded systems- control system and industrial automation- biomedical-data communication system- network information appliances- IVR systems- GPS systems.

UNIT II DEVELOPMENT OF SOFTWARE ARCHITECTURE

Development of software architecture – simple round robin architecture- design and implementation of digital multimeter- round robin with interrupt architecture- implementation of communication bridge- function queue scheduling architecture- RTOS architectur.

UNIT III HARDWARE ARCHITECTURE

Hardware architecture- block schematic of a typical hardware architecture- CPU-memory-I/O Devices- design with microprocessors development- ADC- DAC interfacing LED/LCD interfacing. Case study of processor- 16 bit and 32 bit processor-DSP processor.

UNIT IV EMBEDDED SYSTEM PLATFORM AND DEVELOPMENT TOOLS

Inter process communication- UART-IEEE 1394-IRDA-USB-PCI development tools- EPROM ERASER-signature validator- accelerated design for video accelerator.

UNIT V OVERVIEW OF DESIGN TECHNOLOGIES

Design methodologies and tools- designing hardware and software components- system analysis and architecture design- system integration- structural and behavioral description smart cards.

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice. 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I IMPORTANT PARAMETERS GOVERNING THE HIGH SPEED PERFORMANCE OF DEVICES AND CIRCUITS

10 hrs.

Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature. Contact resistance and interconnection/interlayer capacitances in the Integrated Electronics Circuits.

Materials for high speed devices and circuits: Merits of III – V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs etc.), silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices. Brief outline of the crystal structure, dopants and electrical properties such as carrier mobility, velocity versus electric field characteristics of these materials. Material and device process technique with these III-V and IV – IV semiconductors.

UNIT II METAL SEMICONDUCTOR CONTACTS AND METAL INSULATOR SEMICONDUCTOR AND MOS DEVICES

10 hrs.


Metal semiconductor Field Effect Transistors (MESFETs): Pinch off voltage and threshold voltage of MESFETs. D.C. characteristics and analysis of drain current. Velocity overshoot effects and the related advantages of GaAs, InP and GaN based devices for high speed operation. Sub threshold characteristics, short channel effects and the performance of scaled down devices.

UNIT III HIGH ELECTRON MOBILITY TRANSISTORS (HEMT)

10 hrs.

Hetero-junction devices. The generic Modulation Doped FET(MODFET) structure for high electron mobility realization. Principle of operation and the unique features of HEMT. InGaAs/InP HEMT structures.

Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high speed applications. GaAs and InP based HBT device structure and the surface passivation for stable high gain high frequency performance. SiGe HBTs and the concept of strained layer devices.

UNIT IV INTRODUCTION TO MATLAB

10 hrs.


UNIT V ARRAYS, FUNCTIONS & FILES AND PLOTTING

10 hrs.

Columns and rows: creation and indexing, Size & length, Multiplication, division, power, Operations Writing script files: Logical variables and operators, Flow control, Loop operators, Writing functions: Input/output arguments, Function visibility, path. Example: Matlab startup. Basic 2D plots, XY-plotting functions, Subplots and Overlay plots, Special Plot types, Interactive plotting, Function Discovery, Regression, 3-D plots.

TEXT BOOKS:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80

Exam Duration: 3 hrs.

Part A: 6 Questions of 5 marks each – No choice 30 marks

Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I FUNDAMENTALS OF ANN  

UNIT II ANN ALGORITHM  

UNIT III APPLICATION OF ANN  

UNIT IV INTRODUCTION TO FUZZY LOGIC  

UNIT V APPLICATION OF FUZZY LOGIC  

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN
Max. Marks: 80  
Exam Duration: 3 hrs.
Part A: 6 Questions of 5 marks each – No choice  
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks  
(Distribution may be 80% Theory & 20% Problem)
UNIT I INTRODUCTION TO ASICS, CMOS LOGIC 


UNIT II ASIC TECHNOLOGY 

ASIC library design - Cell design - Architecture - Gate array design - PLDs and FPGAs - ASIC families. CAD for ASIC design - Design entry - VHDL/Verilog - Netlist extraction

UNIT III PROGRAMMABLE ASICS 

Anti fuse – static RAM –EPROM and EEPROM technology- PREP benchmarks-Actel ACT- Xilinx LCA –Altera MAX DC & AC inputs and outputs-Clock & Power inputs- Xilinx i/o blocks.

UNIT IV DESIGN AUTOMATION TOOLS & ALGORITHMS 


UNIT V TESTING 

Design for testability – Application Examples for ASICs: Low noise audio circuit, DC-DC converter - Case study: ARM Processor.

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I FUNDAMENTAL CONCEPTS AND MODELING IN VHDL-AMS


UNIT II DIGITAL MODELING CONSTRUCTS IN VHDL-AMS


UNIT III ANALOG MODELING CONSTRUCTS IN VHDL-AMS


UNIT IV INTRODUCTION TO SYSTEM VERILOG


UNIT V INTERPROCESS SYNCHRONIZATION & COMMUNICATION IN SYSTEM VERILOG


TEXT BOOKS:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80
Exam Duration: 3 hrs.
Part A: 6 Questions of 5 marks each – No choice
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks

M.Tech (VLSI DESIGN) 19 REGULATIONS 2010
UNIT I EMI ENVIRONMENT

Introduction to EMI/EMC-Basics of electro Magnetic interference(EMI)Fundamentals of electromagnetic compatibility(EMC)-Radiation hazards Transients and other EMI sources Transients Electrostatics discharge(ESD)-Tempest- Lightning – Standards of EMI

UNIT II EMI COUPLING

EMI from apparatus and circuits: Introduction-Electromagnetic emission-Appliances-noise from relays and switches-nonlinearities in circuits-Passive inter modulation-Cross talk in transmission lines-Transmission in power supply lines-Electromagnetic interference.

UNIT III EMI SPECIFICATION/STANDARDS AND MEASUREMENTS

Units of specification-civilian standards and military standards.Basics of EMI measurements-EMI measurement tools-TEMcell-measurement using TEM cell-Reverberating chamber-GTEM cell-Anechoic chamber-Open area test site-RF absorbers-conducted interference measurements-conducted EMI from equipments-Experimental setup for measuring conducted EMI-Measurement of DM interferences.

UNIT IV EMI CONTROL TECHNIQUE

Shielding technique-Filter techniques-Grounding techniques-Bonding techniques-Cable connectors and components-Isolation transformer-Transient suppressor

UNIT V EMC DESIGN OF PCB

Designing for EMC:Introduction-Different techniques involved in designing for EMC-EMC guide lines for PCB designs-EMC design guide line for audio and control circuit design-EMC guide lines for RF design-EMC guidelines for power supply design-Mother board designs and propagation delay performance models

TEXT BOOK:

REFERENCES BOOKS:
2. DonWhite consultant incorporate-Handbook of EMI/EMC- Vol 1-1985

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80
Exam Duration: 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I FUNDAMENTALS OF PROGRAMMABLE DSP'S

10 hrs.

UNIT II TMS320C5X PROCESSOR

10 hrs.
Architecture – Assembly Language syntax- Addressing modes- Assembly language Instructions – pipeline structure, Operation – Block diagram of DSP Starter kit – Application Programs for processing real time signals.

UNIT III TMS320C3X PROCESSOR

10 hrs.
Architecture – Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences , Filter design.

UNIT IV ADSP PROCESSORS

10 hrs.
Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

UNIT V ADVANCED PROCESSORS

10 hrs.

TEXT BOOK:

REFERENCE BOOKS:
1. User guides Texas Instrumentation, Analog Devices, Motorola.

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80  
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I INTRODUCTION

Introduction to Wireless technologies: WAP services, serial and parallel Communication, Asynchronous and synchronous communication, EDM, TFM, Spread spectrum technology

Introduction to Bluetooth: Specification, core protocols, cable replacement protocol

UNIT II BLUETOOTH RADIO AND NETWORKING


UNIT III CONNECTION ESTABLISHMENT PROCEDURE

Connection establishment procedure, notable aspects of connection establishment, Mode of connection, Bluetooth Security, Security architecture, Security level of services, profile and usage model: Generic access profile (GAP), SDA, serial profile, Secondary Bluetooth profile.

UNIT IV HARDWARE

Hardware: Bluetooth implementation, Baseband overview, packet format, Transmission

Buffers, Protocol implementation: link manager protocol, logical link control Adaptation protocol, Host control interface, protocol interaction with layers.

UNIT V APPLICATIONS

Programming with Java: Java Programming, J2ME architecture, Javax, Bluetooth package interface, classes, exceptions, Javax.obex package:interfaces, classes Bluetooth services overview of IRDA, HomeRF, Wireless LANs, JINI

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80 Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES 10 hrs.

Static Random Access Memory (SRAMs): SRAM cell structure-MOS SRAM architecture-MOS SRAM cell and peripheral circuit operation-bipolar SRAM technologies-Silicon on insulator (SOI) technology-advanced SRAM architectures and technologies, application specific SRAMs-CMOS CRAMs - DRAMs cell theory and advanced cell structures-BiCMOS DRAMs-soft error failure in DRAMs -Advanced DRAM designs and architecture-application specific DRAMs.

UNIT II NONVOLATILE MEMORIES 10 hrs.

Masked Read-only memories (ROMs) : High density ROMs-Programmable read only memories(PROMs) - Bipolar PROMs- CMOS PROMs-erasable(UV)- Programmable read only memories (EPROMs)-Floating Gate EPROM-cell-one -time programmable (OTP) EPROMs-Electrically Erasable PROMs(EEPROMs)- EEPROM technology and architecture-nonvolatile SRAM-Flash memories(EPROMs or EEPROM)-Advanced flash memory architecture.

UNIT III ADVANCED MEMORY TECHNOLOGIES AND HIGH -DENSITY MEMORY PACKAGING TECHNOLOGIES 10 hrs.

Ferroelectric Random Access Memories(FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog memories magnetoresistive random access memories(MRAMs) – Experimental memory devices.

Memory hybrids and MCMs(2D)-Memory stacks and MCMs (3D)-Memory MCM testing and reliability issues-memory cards-high density memory packaging future directions.

UNIT IV SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS 10 hrs.

General Reliability issues-RAM failure modes and mechanism-nonvolatile memory reliability-reliability modeling and failure rate prediction- design for reliability-reliability test structures-reliability screening and qualification. Radiatoneffects-single event phenomenon(SEP)-radiation hardening techniques-radiation hardening process and design issues-radiation hardened memory characteristics-radiation hardness assurance and testing-radiation dosimetry - water level radiation testing and structures.

UNIT V MEMORY FAULT MODELING,TESTING AND MEMORY DESIGN FOR TESTABILITY AND DAULT TOLERANCE 10 hrs.

RAM fault modeling,electrical testing,Pseudo random testing-megabit DRAM-nonvolatile memory modeling and testing-IDDQ fault modeling and testing-application specific memory testing and the tools for fault modeling and testing

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80 Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I INTRODUCTION & MATHEMATICAL FOUNDATION

Beginning with a simple communication game – wrestling between safeguard and attack – Probability and Information Theory - Algebraic foundations – Number theory.

UNIT II ENCRYPTION – SYMMETRIC TECHNIQUES


UNIT III ENCRYPTION – ASYMMETRIC TECHNIQUES & DATA INTEGRITY TECHNIQUES


UNIT IV AUTHENTICATION


UNIT V SECURITY PRACTICES


TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice  30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks  50 marks
UNIT I


UNIT II

Receiver Front End – Motivations - General Design Philosophy- Heterodyne and Other architectures - Filter Design - Band Selection Filter – Image Rejection Filter - Channel Filter - Non idealities and Design Parameters - Harmonic Distortion – Intermodulation -Cascaded Nonlinear Stages – Gain Compression – Blocking – Noise - Noise Sources -Noise Figure - Design of Front end parameter for DECT.

UNIT III


UNIT IV


UNIT V


TEXT BOOK:

REFERENCE BOOKS:
UNIT I RF ELECTRONIC CONCEPTS

Introduction – RF Microwave Vs DC or AC signals – Importance of radio frequency design – RF behaviour of passive components – High frequency resistors - High frequency capacitors - High frequency inductors – Chip components – Circuit board consideration – Chip resistors-Chip capacitors-Surface mounted inductors- resonant circuits – Analysis of a simple circuit and Phasor domain – Impedance transformation – Insertion loss- Impedance transformers-RF impedance matching. BJT and MOSFET behavior at RF.

UNIT II SMITH CHART


UNIT III MATCHING AND BIASING NETWORK


UNIT IV DESIGN OF AMPLIFIERS

Stability considerations in active network – Gain considerations in amplifiers – Power gain concepts – Unilateral transistor – Mismatch factor – Input &output VSWR – Maximum gain design – Constant gain circles – Unilateral figure of merit – Bilateral case – Amplifiers RF circuit design –Design of different types of amplifiers –Narrow band amplifier design – High gain amplifier design – Maximum gain amplifier design – Low noise amplifier design -Maximum noise amplifier design –Broad band amplifier design- Multistage small signal amplifier design –High power amplifier –Large signal amplifier design - Integrated RF Filters,

UNIT V RF MICROWAVE OSCILLATOR DESIGN


TEXT BOOKS:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
(Distribution may be 50% Theory & 50% Problem)
UNIT I THEORY OF PARALLELISM  
10 hrs.
Parallel computer models-the state of computing, multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks.

UNIT II APPLICATIONS  
10 hrs.
Programs and network properties-conditions of parallelism, Program partitioning and scheduling, program flow mechanisms, system interconnect architectures, principles of scalable performance matrices and measures, parallel processing applications, speed up performance laws, scalability analysis and approaches.

UNIT III HARWARE TECHNOLOGIES  
10 hrs.
Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory-backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.

UNIT IV PIPELINING AND SUPER SCALAR TECHNOLOGIES  
10 hrs.
Parallel and scalable architectures, Multiprocessor and multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architecture.

UNIT V SOFTWARE AND PARALLEL PROGRAMMING  
10 hrs.
Parallel models, Languages and compilers, Parallel program development environments, UNIX, MACH and OSF/1 for parallel computers.

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN
Max. Marks: 80
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I INTRODUCTION

Introduction-modeling basic analog concepts-analog circuit analysis-network independent-dependence data sampled analog systems, loading.

UNIT II VHDL APPLICATION TO ANALOG AND MIXED SIGNAL EXTENSIONS

Introduction-language design objectives-Theory of differential algebraic equation-the 1076.1 language-tolerance groups-conservative systems-time and the simulation cycle-A/D and D/A interaction-Question point-frequency domain modeling and examples.

UNIT III ANALOG EXTENSIONS TO VERILOG


UNIT IV BEHAVIORAL GENERIC MODEL OF OPERATIONAL AMPLIFIERS


UNIT V NON-LINEAR STATE SPACE AVERAGED MODELING OF 3-STATE DIGITAL PHASE-FREQUENCY DETECTOR

Introduction-modeling of multi state phase frequency detector-resetable integrator-AC analysis-sample application.

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80 Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I  
Clocked logic styles, single-Rail Domino logic styles, Dual-Rail Domino structures, Latched Domino structures, clocked pass gate logic, Non-clocked logic styles, Static CMOS, DCVS logic, Non-clocked pass gate families.

UNIT II  
Circuit design Margining, Design induced Variations, process induced Variations, Application induced Variations, Noise.

UNIT III  
Latching strategies, Basic Latch Design, Latching Differential logic, Hazards, Race Free Latches for Pre-charged logic, Asynchronous latch techniques.

UNIT IV  
Signaling standards, chip-to-chip communication Networks, ESD Protection, Standards and Models with design -Skew Tolerant design.

UNIT V  
Clocking styles, clock jitter, signal skew, clock skew, and data feed through clock generation, clock distribution, and asynchronous clocking techniques.

TEXT BOOK:

REFERENCES BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN
Max. Marks: 80  
Exam Duration : 3 hrs.
Part A: 6 Questions of 5 marks each – No choice  
30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks  
50 marks
UNIT I INTRODUCTION TO NANOTECHNOLOGY

Nanoscale technology: Consequences of the nanoscale for technology and society. Beyond Moore’s Law. Molecular building blocks for nanostructure systems, Nano-scale 1D to 3D structures,

Energy Band Diagram: Energy level diagram, Fermi function, n-type operation, p-type operation, Rate equations for a one-level model, Current in a one-level model, Inflow / Outflow, Pauli blocking, quantum of conductance, Potential profile, Iterative procedure for self-consistent solution, Quantum capacitance, Negative Differential Resistance (NDR).

UNIT II ELECTRICAL RESISTANCE-AN ATOMISTIC VIEW


UNIT III MOLECULAR ELECTRONIC DEVICES

Basic Concepts- Self assembled Layers, Charge transport Mechanisms; Synthesis of Molecular wires and devices synthesis of two terminal devices, Fabrication of molecular transport devices; Simple SAM metal-insulator-metal Tunneling.

UNIT IV NANOSCALE DEVICE MODELING

Inadequacy of macroscopic models, Equilibrium, Non-Equilibrium, Density Matrix and current operator; NEGF Formalism – Broadening.

UNIT V NANOSCALE DEVICE MODELING

Quantum Point Contact- Hamiltonian, Self energy; SAM- Signals used to control and probe molecules, Synthesis; Fabrication and overview of Nanotube devices- their properties.

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80 Exam Duration : 3 hrs
Part A: 6 Questions of 5 marks each – No choice 30 marks
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks 50 marks
UNIT I


UNIT II


UNIT III

Sensors for aerospace and defense: Accelerometer, Pressure Sensor, Night Vision System, Nano tweezers, nano-cutting tools, Integration of sensor with actuators and electronic circuitry, Civil applications: metrology, bridges and other industrial applications.

UNIT IV


UNIT V


REFERENCE BOOKS:

UNIT I INTRODUCTION TO DIGITAL SYSTEMS

Analog vs Digital systems, digital devices, integrated circuits, programmable logic devices, digital design levels, software aspects of digital design.

UNIT II LOGIC CIRCUITS


UNIT III SEQUENTIAL LOGIC PRINCIPLES


UNIT IV INTRODUCTION TO PLD'S & MAX PLUS II

Programming PLDs using MAX PLUS II, Graphic Design File, Compiling MAX PLUS II Files, Hierarchical Design.

UNIT V COMBINATIONAL LOGIC DESIGN PRACTICES

Documentation standards, Circuit timing, Combinational PLDs. Design using SSI and MSI devices Decoders, Encoders, Three state buffers, Multiplexers, Parity circuits, Comparators, Adders, Subtractors, ALUs, Combinational multipliers. Using VHDL and PLDs Combinational circuit design examples – barrel shifter, simple floating – point encoder, cascading comparator.

TEXT BOOK:

REFERENCE BOOKS:

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UNIT I METHODS FOR COMBINATIONAL OPTIMIZATION  


UNIT II CLUSTERING  

Layout Compaction, Placement, Floor planning And Routing Problems, Rajaraman and Wong Algorithm, Flow Map Algorithm, Multi-Level Coarsening Algorithm.

UNIT III PARTITIONING & FLOOR PLANNING  

Kernighan and Lin Algorithm, Fiduccia and Mattheyses Algorithm, EIG Algorithm, FBB Algorithm.

Floorplanning algorithms - Stockmeyer Algorithm, Normalized Polish Expression, ILP Floor planning Algorithm, Sequence Pair Representation.

UNIT IV PLACEMENT & ROUTING  


UNIT V PHYSICAL DESIGN AUTOMATION OF FPGA’S & MCM’S  

FPGA technologies, Physical Design cycle for FPGA’s, partitioning and routing for segmented and staggered Models. MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches.

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80  
Exam Duration : 3 hrs.

Part A: 6 Questions of 5 marks each – No choice  
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks
UNIT I INTRODUCTION TO HIGH-LEVEL SYNTHESIS

System-Level Design of Hardware Systems - Overview of High-Level Synthesis - Role of Parallelizing Compiler Transformations in HLS - HLS for Behaviors with Complex Control Flow - Intermediate Representations in High-Level Synthesis - Use of Loop Transformations in Compilers and High-Level Synthesis

UNIT II MODELS AND REPRESENTATIONS


UNIT III PARALLELIZING HIGH-LEVEL SYNTHESIS


UNIT IV CODE TRANSFORMATIONS AND SCHEDULING


UNIT V SPARK: IMPLEMENTATION, SCRIPTS AND DESIGN EXAMPLES

Implementation of the SPARK PHLS Framework - Command-line Options and Scripts in SPARK - Interdependencies between the Code Motions - Enabling and Disabling One Code Motion at a Time - Enabling Multiple Code Motions at a Time - Ways of Calculating Priority - Design Examples - Study of Loop Unrolling and Loop Shifting - Synthesis of an Instruction Length Decoder

TEXT BOOK:

REFERENCE BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

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UNIT I INTRODUCTION

Typical uses of Perl – Event driven Simulators -Perl -Perl philosophy - A Perl program-Three virtues of a programmer - Parts of Perl - The Perl interpreter - Manuals/Documentation-Perl Modules - Perldoc: Using perldoc - Other ways to access perldoc - Creating and running a Perl program: Perl program- Running a Perl program from the command line Executing code-The "shebang" line for Unix-The "shebang" line for non-Unixes -Command line options and warnings-Lexical warnings.

UNIT II VARIABLES AND ARRAYS

Perl variables- Special characters - Advanced variable interpolation- Arrays-Initializing an array-Reading and changing array values -Array slices - Array interpolation Counting backwards - Finding out the size of an array -Printing out the values in an array-Hashes -Initializing a hash-Reading hash values -Adding new hash elements -Changing hash values-Deleting hash values-Finding out the size of a hash -Other things about hashes-Special variables.

UNIT III OPERATORS AND FUNCTIONS

Operators- Arithmetic operators-String operators-Other operators –Functions-Types of arguments-Return values -Some easy functions-String manipulation-Finding the length of a string-Case conversion -Type conversions -Manipulating lists and arrays-push, pop, shift and unshift -Ordering lists-Converting strings to lists.

UNIT IV CONDITIONAL CONSTRUCTS

The if conditional construct -Comparison operators -Existence and definitiveness-boolean logic operators -Logic operators and short circuiting -Boolean assignment -Loop conditional constructs -while loops-for and foreach-Practical uses of while loops: taking input from STDIN -Named blocks-Breaking out or restarting loops-Smart-match-given and when.

UNIT V SUBROUTINES AND REGULAR EXPRESSIONS

Subroutines: Introducing subroutines-Using subroutines in Perl.-Calling a subroutine- Passing arguments to a subroutine -Passing in scalars -Passing in arrays and hashes-Returning values from a subroutine -Regular expressions -Regular expression operators and functions-m/PATTERN/ - the match operator -s/PATTERN/REPLACEMENT/ - the substitution operator-Binding operators -Easy modifiers -Meta characters -Some easy meta characters-Quantifiers -Grouping techniques -Character classes -Alternation-The concept of atoms.

TEXT BOOK:

REFERENCES BOOKS:

UNIVERSITY EXAM QUESTION PAPER PATTERN

Max. Marks: 80

Part A: 6 Questions of 5 marks each – No choice
Part B: 2 Questions from each unit of internal choice, each carrying 10 marks

Exam Duration : 3 hrs.

30 marks

50 marks
UNIT I INTRODUCTION

UNIT II MICRO SENSING FOR MEMS
Piezoresistive sensing - Capacitive sensing - Piezoelectric sensing - Resonant sensing - Surface acoustic wave sensors.

UNIT III MICRO MACHINING AND LITHOGRAPHY

UNIT IV MEMS INDUCTORS AND CAPACITORS

UNIT V APPLICATIONS

TEXT BOOK:

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